1. (Amended) A method of improving the SiGe bipolar yield of a SiGe heterojunction bipolar transistor comprising the steps of:

providing a heterojunction bipolar transistor structure comprising at least an underlying SiGe base region, an insulator layer formed on surface portions of said underlying SiGe base region, and an emitter formed on said insulator layer and in contact with said underlying SiGe base region through an emitter opening formed in said insulator layer, said emitter, said insulator layer and said SiGe base region each having exposed sidewalls;

forming a passivation layer on said exposed sidewalls of said emitter, said insulator layer and portions of said SiGe base region; and

siliciding exposed silicon surfaces of at least said emitter and said SiGe base region not protected by said passivation layer to form silicide regions therein.

7. (Amended) The method of Claim 2 wherein said rapid thermal chemical vapor deposition process is carried out at a temperature of about 700°C or greater.

9. (Amended) A SiGe heterojunction bipolar transistor comprising:

a semiconductor substrate having a collector and subcollector region located therein, wherein said collector is located between isolation regions that are also present in the substrate;

a SiGe layer atop said substrate, said SiGe layer including polycrystalline Si regions positioned above said isolation regions and a SiGe base region located above said collector and subcollector regions;

a patterned insulator layer atop said SiGe base region, said patterned insulator having an opening therein;

an emitter located on said patterned insulator layer and in contact with said SiGe base region through said opening, said emitter, said patterned insulator layer and said SiGe base region each having exposed sidewalls;

a conformal passivation layer positioned on said exposed sidewalls of said emitter, said patterned insulator layer and said SiGe base region; and

silicide regions located on exposed portions of said SiGe layer and said emitter not covered by said conformal passivation layer.

REMARKS

Favorable reconsideration and allowance of the claims of the present application are respectfully requested.

Before addressing the specific grounds of rejection raised in the present Office Action, applicants have amended Claims 1, 7 and 9 in the manner indicated supra. Specifically, applicants have amended Claim 1 to positively recite the processing steps which are depicted in FIGS 2-8 where a heterojunction bipolar transistor structure comprising at least an underlying SiGe base region, an insulator layer formed on surface portions of said underlying SiGe base region, and an emitter formed on said insulator layer and in contact with said underlying SiGe base region through an emitter opening formed in said insulator layer, said emitter, said insulator layer and said SiGe base region each having exposed sidewalls, is provided prior to forming a passivation layer on the exposed sidewalls of the emitter, insulator layer and portions of the SiGe base region (FIG 8) and silicidation (FIG 2). In addition to